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10ES32

Third Semester B.E. Degree Examination, June/July 2016

Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain Reverse recovery time of a semiconductor diode. **(06 Marks)**

b. The Fig. Q1 (b) shows two way clipper. Determine its output wave form. Assume diode drop of 0.7V. **(07 Marks)**

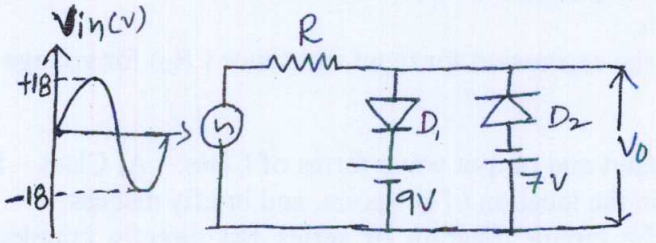


Fig. Q1(b)

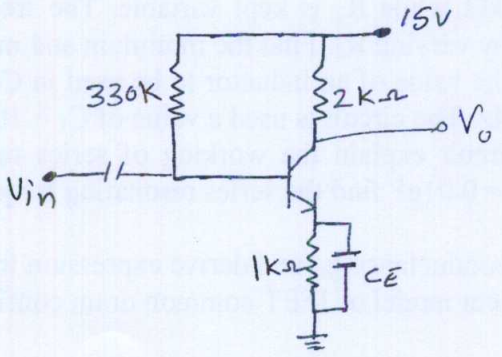
c. What is clamper circuit? Explain the operation of Positive and Negative clamper circuits and draw the wave form. [Assume Ideal Diode]. **(07 Marks)**

2 a. What is transistor biasing? Discuss the causes of bias instability in a transistor. **(06 Marks)**

b. Derive the expression for I_B, V_{CE} and $S(I_{CO})$ for voltage divider bias using exact analysis. **(07 Marks)**

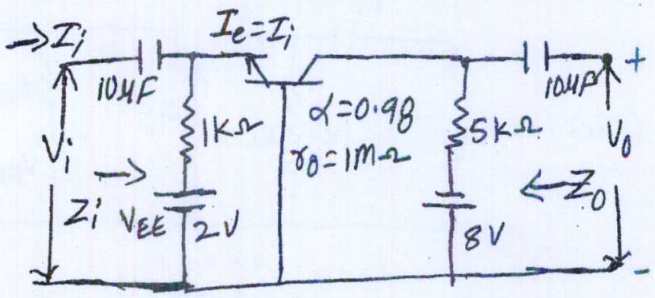
c. For the circuit shown in Fig. Q2(c). Find I_B, I_C, V_{CE}, V_C and V_E. Assume $\beta = 100$, VBE = 0.7. **(07 Marks)**

Fig. Q2(c)



3 a. For common base configuration shown in Fig Q3(a). Find r_e, z_i, z_o and A_v. **(06 Marks)**

Fig. Q3(a)



b. Derive an expression for z_i, z_o, A_V and A_i of a CE fixed bias configuration using r_e model. **(07 Marks)**

c. Using h-parameter model for a transistor in C.E configuration. Derive expressions for A_I, z_i and A_v. **(07 Marks)**

4 a. An amplifier consists of 3 identical stages in cascade; the bandwidth of overall amplifier extends from 20Hz to 20KHz. Calculate the band width of Individual stage. **(06 Marks)**

b. Describe miller effect and derive an equation for miller input and output capacitance. **(07 Marks)**

c. Draw and explain frequency response of an amplifier and briefly discuss the effect of various capacitors on frequency response. **(07 Marks)**

PART – B

5 a. Explain the need of cascade amplifier and list the advantage of this circuit. **(06 Marks)**

b. With block diagram, explain the concept of feedback. List the advantages of negative feedback. **(07 Marks)**

c. Derive the expression for input resistance (R_{if}) for voltage series feedback amplifier. **(07 Marks)**

6 a. Draw input and output wave forms of Class – A, Class – B and Class – C power amplifiers based on the location of Q - point, and briefly discuss. **(06 Marks)**

b. Draw the circuit diagram of series fed directly coupled Class – A amplifier. Give the expression for dc power input and a.c power output and show that efficiency is 25%. **(07 Marks)**

c. What is Harmonic distortion? Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5V second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05V. Also calculate the total harmonic distortion. **(07 Marks)**

7 a. With neat circuit diagram explain the operation of BJT Hartley oscillator. **(06 Marks)**

b. i) The frequency sensitive arms of the wien bridge oscillator uses $C_1 = C_2 = 0.001\mu F$ and $R_1 = 10k\Omega$ while R_2 is kept variable. The frequency is to be varied from 10KHz to 50KHz by varying R_2. Find the minimum and maximum values of R_2.

ii) Design the value of an inductor to be used in Colpitts oscillator to generate a frequency of 10MHz. The circuit is used a value of $C_1 = 100pF$ and $C_2 = 50pF$. **(07 Marks)**

c. With neat circuit explain the working of series resonant crystal oscillator. A crystal has L = 0.1H, C = 0.01pF find the series resonating frequency. **(07 Marks)**

8 a. Define transconductance g_m and derive expression for gm. **(06 Marks)**

b. With equivalent model of JFET common drain configuration. Obtain the expression for z_i, z_o and A_v. **(07 Marks)**

c. For common gate amplifier as shown in Fig Q8.(c), gm = 2.8ms, $r_d = 50k\Omega$ Calculate z_i, z_o and A_v. **(07 Marks)**

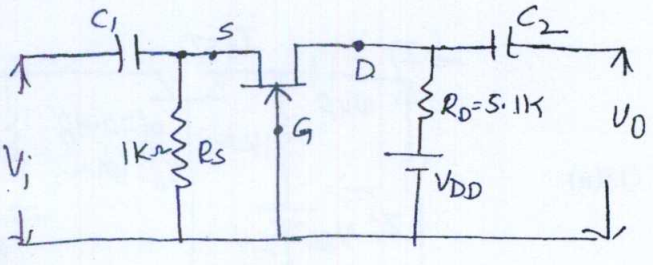


Fig. Q8(c)

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